LEARNING ELECTRONIC CIRCUITS USING *MULTISIM*: A CASE STUDY – THE DARLINGTON AMPLIFIER

Luiz C. M. Torres[1] ; Denise Consonni[2]
Escola Politécnica da USP, Depto. De Engenharia de Sistemas Eletrônicos
Av. Prof. Luciano Gualberto, tv.3, N.158
CEP 05508-900, São Paulo, SP, Brasil
[1]molina@lme.usp.br; [2]dconsoni@lme.usp.br

Abstract: *The objective of this work is to illustrate to second year Electrical Engineering students the importance of using a simulation software, such as* ***Multisim*** *[1], in order to learn faster and to better understand the procedures involved with the design and analysis of electronic circuits. As a case study, we present the Darlington Amplifier [2], introducing bipolar junction transistor (BJT) as current amplifiers and employing well-known models to explain their operation. The analysis starts by obtaining the circuit operating bias point, from a circuit schematics composed with* ***Multisim*** *library components, including BJT non-linear models. The transfer curve (voltage output versus input current) is traced, by DC sweeping the input current source around the quiescent point. On this characteristic curve, the student can easily visualize the potential linear and non-linear regions of circuit amplification. Using the BJT model parameters determined at bias point, linear DC models are built to replace the transistors in circuit schematics, and the transfer curve is again obtained. Its unreal linear shape is superimposed and compared to the former characteristic. An AC analysis is then performed, using the original* ***Multisim*** *BJT models: magnitude and phase AC amplifier responses are calculated, as the input signal frequency is varied. Again from the bias point results, π-hybrid BJT model [2] parameters are extracted and the AC analysis is repeated inserting these models into the amplifier schematics. AC frequency performance is then compared to the previous responses. The Transient analysis is very useful to demonstrate the effects produced by device non-linearity and input signal level and frequency on the amplifier output voltage. Finally, the Fourier and Distortion analyses produce useful practical results for amplifier design purposes.*

Key-words: *Electronic circuits, Multisim, Darlington amplifier, Simulation*

1. DARLINGTON AMPLIFIER SCHEMATICS

Figure 1 shows the amplifier circuit as seen in the ***Multisim*** schematic capture stage, where BJTs Q_1 and Q2 are arranged in a Darlington configuration which produces amplification of the input current signal represented by IENT, extracted at the circuit output voltage, named VS. PN2222 and PN2907A are components of the ***Multisim*** *Master Database*, *Transistors Group*, *BJT_NPN* and *BJT_PNP Families* respectively. Circuit biasing is provided by the 6V DC V1 voltage source.

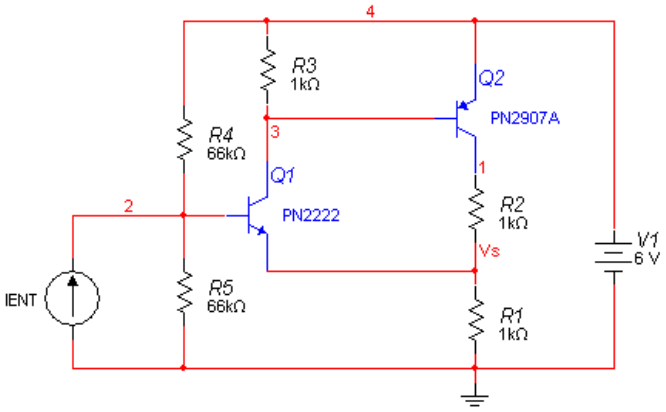

Figure 1- Darlington Amplifier Circuit

The Darlington amplifier is used to introduce the bipolar transistor as an amplification element to our Electrical Engineering students. It features some interesting characteristics such as a high input impedance and unit voltage gain, which are convenient for understanding small-signal amplifier response. As a consequence of the high input impedance of the Darlington module, practically all input current signal feeds the parallel association of the two biasing resistors R_4 and R_5 (resulting in this case an equivalent resistance of 33kΩ), generating the input voltage to Q1, which is transferred to the output VS with unit gain. Therefore the amplifier transresistance (ratio between output voltage variation and input current variation) approximates the circuit equivalent input resistance, which is 33kΩ in the schematics shown in Figure1.

2. BIAS OPERATING POINT AND DC TRANSFER CHARACTERISTIC

Determination of the transistors' operating point (also named quiescent point or bias point) is the first thing to do when one is analyzing an amplifier circuit. ***Multisim*** performs this simulation in the *DC Operating Point* analysis, using a nonlinear Ebers-Moll based model [3]. In this type of analysis, the program assumptions are that all AC sources are null, capacitors are replaced by zero-current elements (open circuit) and inductors are substituted by zero-voltage elements (short circuit). The results of this simulation are all the DC node voltages, the collector and base currents, the base-emitter voltages, the collector-base voltages and the small-signal parameters for the BJT at the corresponding bias point set by the DC sources. Variables of the circuit and device/model parameters of interest can be chosen in the *DC Operating Point* analysis window at the *Output Tab*. Table 1 shows the results of DC operating point (calculated for IENT=0), produced by the 6V voltage source of Figure 1.

On the left side of Table 1, V(1), V(2), V(3), V(4) and V(vs) are node voltages, I(q1[ic]) and I(q2[ic]) are the collector currents I_C, I(q1[ib]) and I(q2[ib]) are the base currents I_B, @qq1[vbe] and @qq2[vbe] are the base-emitter voltages V_{BE} and finally @qq1[vbc] and @qq2[vbc] are the base-collector voltages V_{BC} (all DC values) for Q1 and Q2 respectively. On the right side of the same Table are the small-signal parameters of the bipolar transistors. Results from Table 1 used on *Postprocessor Window* enable entering expressions such as, I_C/I_B and gm/gpi, in order to calculate respectively DC and AC transistor current gains at the quiescent point, as shown in Table 2. These parameters will be used in the next steps of circuit analysis.

Table 1- Results of DC Operating Point Analysis

	DC Operating Point	
1	V(1)	3.64740
2	V(2)	2.83434
3	V(3)	5.26487
4	V(4)	6.00000
5	V(vs)	2.19702
6	I(q1[ic])	741.64281 u
7	I(q1[ib])	5.02005 u
8	@qq1[vbe]	637.27557 m
9	@qq1[vbc]	-2.42984
10	I(q2[ic])	1.45038 m
11	I(q2[ib])	6.48870 u
12	@qq2[vbe]	735.06422 m
13	@qq2[vbc]	-1.61650

	DC Operating Point	
1	@qq1[gx]	100.00000 m
2	@qq1[gpi]	174.05043 u
3	@qq1[gm]	28.59285 m
4	@qq1[go]	9.69977 u
5	@qq1[gmu]	0.16512 p
6	@qq1[cpi]	47.87821 p
7	@qq1[cmu]	4.46045 p
8	@qq2[gx]	100.00000 m
9	@qq2[gpi]	245.49531 u
10	@qq2[gm]	55.99024 m
11	@qq2[go]	12.36296 u
12	@qq2[gmu]	0.28078 p
13	@qq2[cpi]	66.88438 p
14	@qq2[cmu]	7.95152 p

Table 2- DC and AC transistor current gains

DC Operating Point

	BETA DC (Q1)	BETA DC (Q2)	BETA AC (Q1)	BETA AC (Q2)
1	147.7	223.5	164.3	228.1

The DC analysis follows with a *DC Sweep* analysis, in order to obtain the DC amplifier transfer characteristic $V_{(VS)}$ x IENT. On this curve, base-emitter and collector-base voltage variations with IENT for both Q1 and Q2 transistors are also superimposed. The results are shown in Figure 2. It is interesting to notice in Figure 2, the distribution of BJTs operation region as a function of the IENT current source level:

Q_1 is in the cut-off region for IENT lower than approximately – 70μA
Q_2 is in the cut-off region for IENT lower than approximately – 45μA
Q_1 is in the saturation region for IENT higher than approximately 110μA
Q_2 is in the saturation region for IENT higher than approximately 35μA

This means that the bipolar transistors are simultaneously in the active region for IENT varying between – 45μA and 35μA approximately. It can be seen that the strictly linear region of the amplifier DC transfer characteristic (Figure 3) is limited by these values, but the curve can still be considered fairly linear within the broader limits from -70μA and 110μA. The slope of this characteristic in its linear region results in a value equals to 33kΩ, corresponding to the DC transresistance.

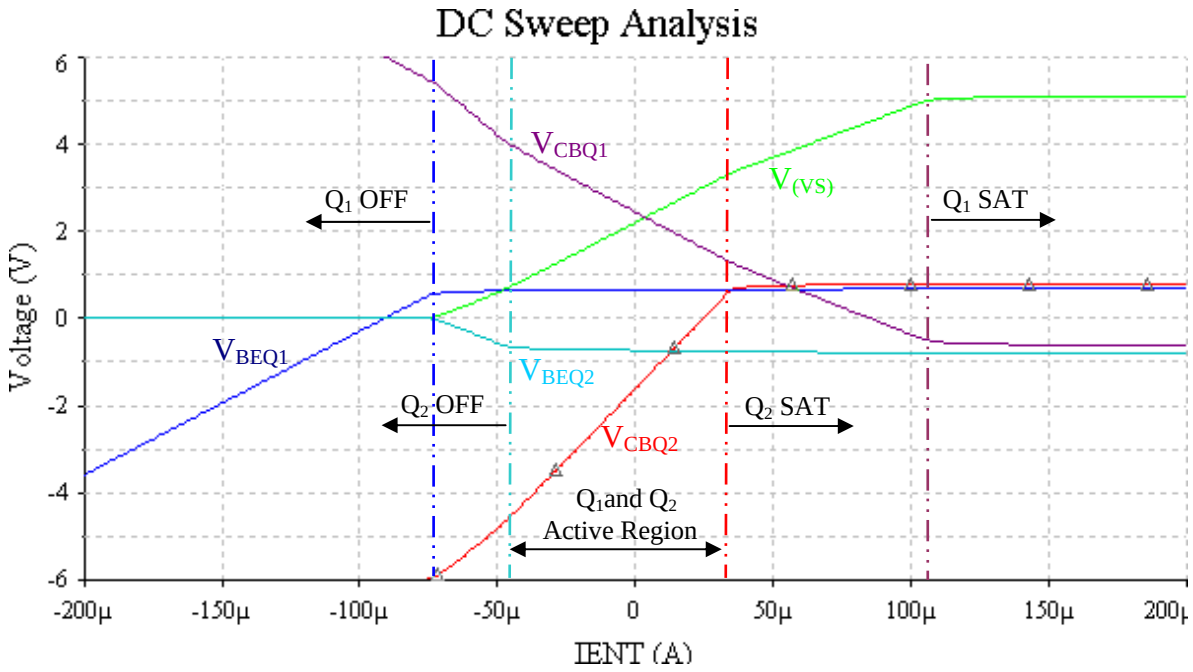

Figure 2- Results of the DC Sweep Analysis

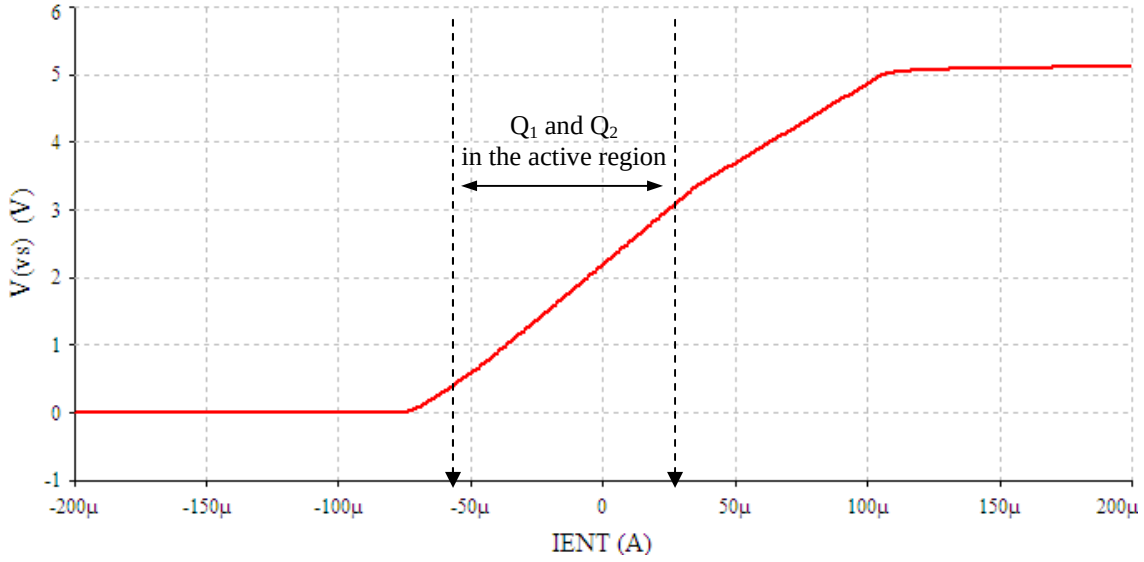

Figure 3- Amplifier DC Transfer Characteristic

3. BJT DC LINEAR MODELING

For a limited range of currents and voltages around the bias point, the highly non-linear operation of BJT devices can be simulated with a linear model as shown in Figure 4. Values of the parameters Rx, V_{BE} and Ro can be taken from Table 1, lines 1 and 8 at the right side, (making Rx = 1/gx), lines 8 and 12 at the left side (V_{BE}) , and lines 4 and 11 at the right side (making Ro = 1/go) for Q_1 and Q_2 respectively. BetaDC values can be extracted from Table 2.

When the bipolar transistors are replaced by the DC linear model of Figure 4, the new schematics of the Darlington Amplifier will result in the circuit shown in Figure 5. Values of V_{BE} in ***Multisim*** are positive for both Q_1 and Q_2, so V_{BE} voltage generator must be placed with the correct polarity in the circuit, in order to represent NPN and PNP structures,

respectively. The controlled current generators inject current from collector to emitter for the NPN BJT and from emitter to collector for the PNP BJT.

The results obtained from the *DC Sweep* analysis of circuit schematics shown in Figure 5, are displayed as a blue trace in Figure 6. For comparison, the red trace refers to the same simulation using non-linear models. As can be seen, a good fit is observed in the region close to the bias point, indicating that the amplifier presents a linear performance while both transistors are operating in the active region. The use of the linear models helps in getting a better visualization of the amplifier linear operation region. However, by comparing both curves, the students should realize the limitations of this simplified linear model and its inability for predicting full-range amplifier performance.

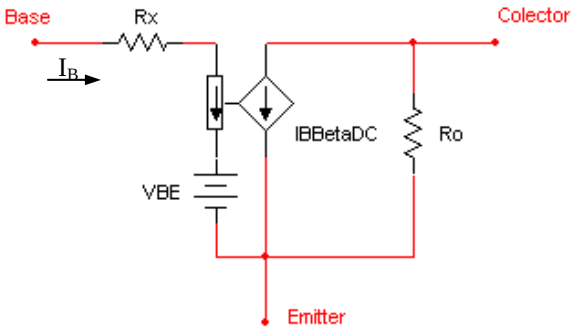

Figura 4- BJT DC Linear Model

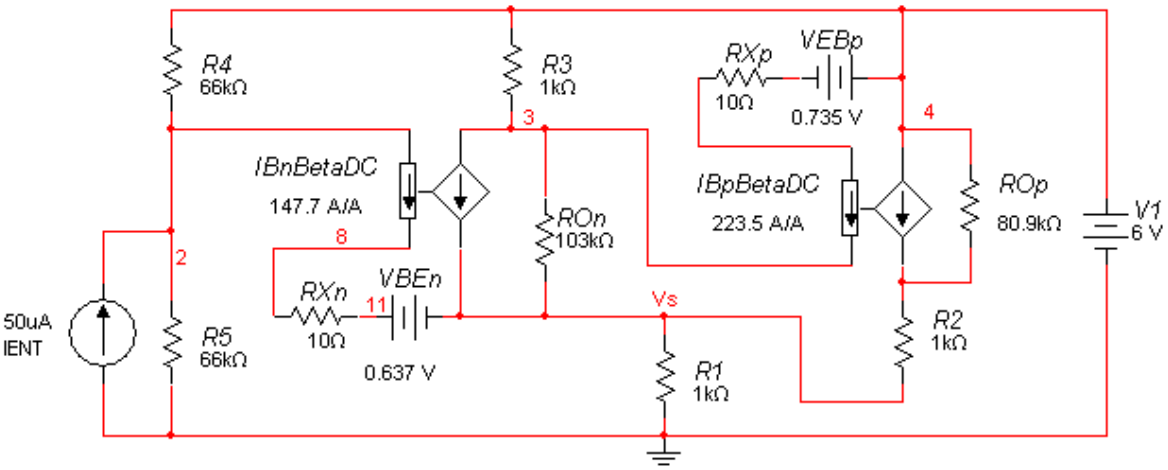

Figure 5- Darlington Amplifier Circuit with BJT DC linear models

4. AMPLIFIER FREQUENCY RESPONSE

The next step is to perform an *AC* analysis in order to investigate the amplifier operation with frequency variation of a sinusoidal input signal. In this simulation, ***Multisim*** uses a BJT AC linear model (π-hybrid model) with the parameters calculated at the bias point. The results obtained are the gain magnitude and phase curves as functions of frequency. The circuit schematics used for this analysis is shown in Figure 7. In Figure 8, the magnitude and phase frequency responses of the amplifier output voltage VS are displayed.

$V_{(VS)}$ - Multisim Non-linear Model
$V_{(VS)}$ - Linear Model

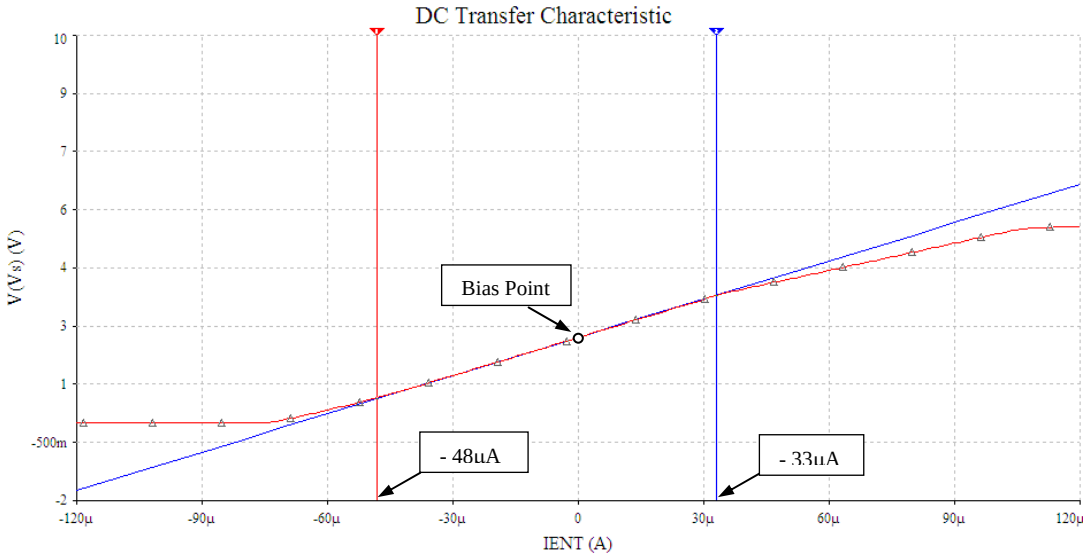

Figure 6- DC Sweep Analysis results for both linear and non-linear models

The amplifier low-frequency transresistance can be obtained from (Vs) low-frequency magnitude (V_{max} indicated by cursor 1 (x_1, y_1) in Figure 8), resulting: V_{max} / IENT = 1.6376 / $5.0x10^{-5}$ = 32.75kΩ, being a good approximation to the initial value (33kΩ), estimated in sections 1 and 2 above. The cut-off frequency can be determined by locating the point where V(Vs) magnitude drops to $V_{max}/\sqrt{2}$ (indicated by cursor 2 (x_2, y_2) in Figure 8), resulting in a value of 1.08MHz approximately. The values of the amplifier transresistance (magnitude and phase) were calculated for other frequencies as listed in Table 3.

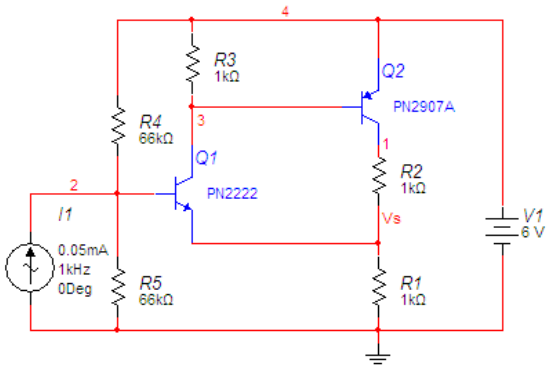

Figure 7- Schematics for AC Analysis

5. BJT π-HYBRID MODEL

In order to introduce to the students the BJT small signal (incremental) model, the *AC* analysis is repeated, replacing each BJT for its corresponding AC model, shown in Figure 9. The resulting circuit can be seen in the schematics of Figure 10. The values for the model parameters were obtained from the DC operating point (at the right side of the Table 1, making rx = 1/gx , rpi = 1/gpi and ro = 1/go) for both NPN and PNP transistors. The results from this AC analysis are shown in Figure 11. Transresistance values resulting from this simulation are listed in Table 4.

A great similarity between the results obtained in sections 4 and 5 can be observed, by comparing Figures 8 and 11, and Tables 3 and 4 .

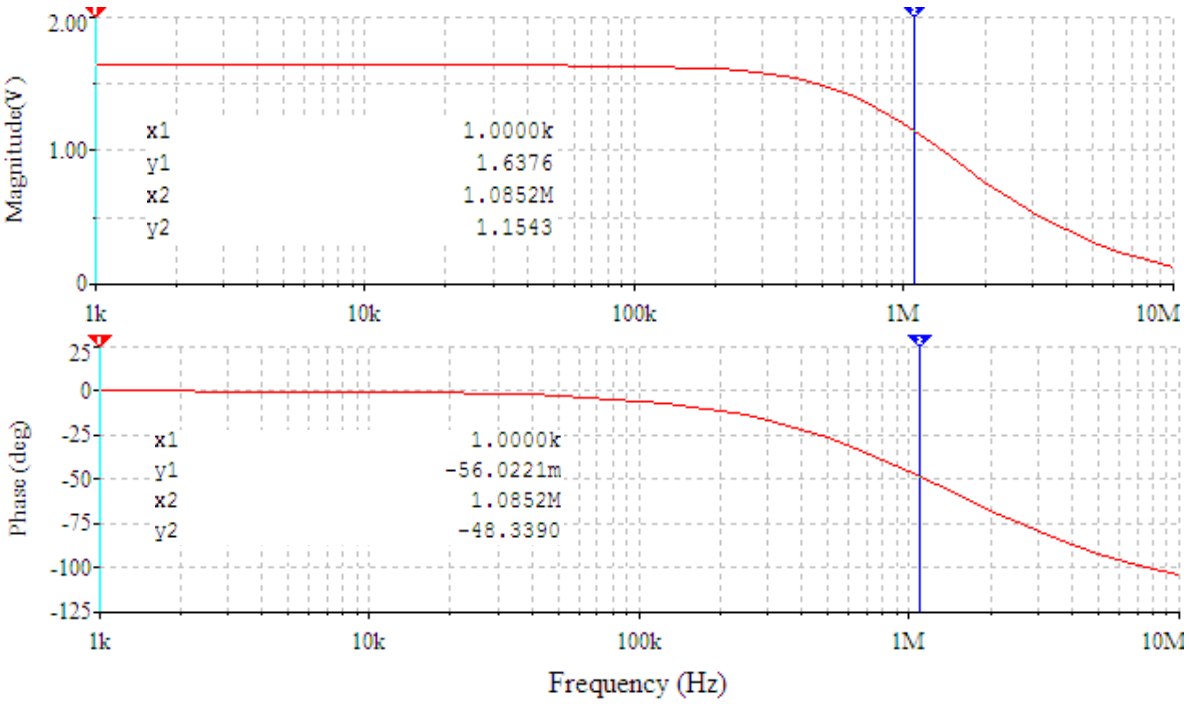

Figure 8 - Amplifier frequency response (VS) as resulted from AC analysis

Table 3 - Transresistance values

Transresistance		
Frequency (kHz)	Magnitude (kΩ)	Phase (degrees)
1	32.75	- 0.056
10	32.75	- 0.56
100	32.61	- 5.59
1,000	23.94	- 46.03
10,000	2.61	- 104.07

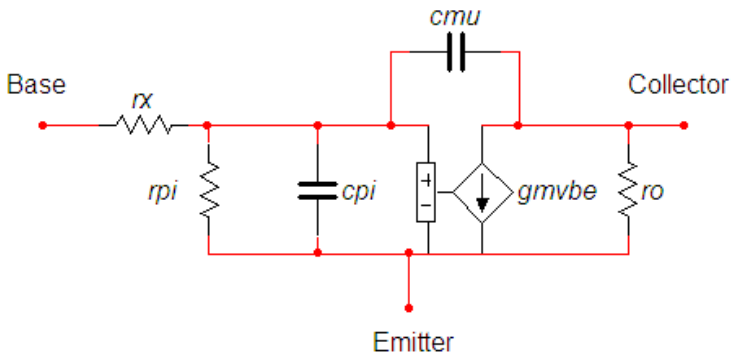

Figure 9- BJT AC model

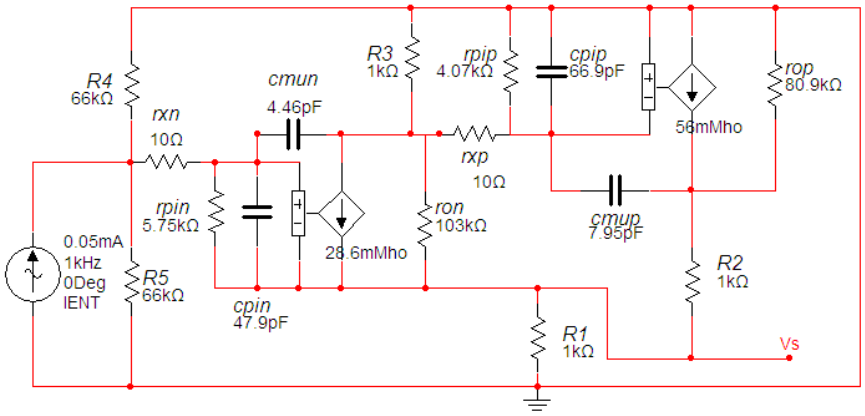

Figure 10 - Darlington Amplifier with BJTs replaced by their incremental model (*n* index refers to NPN transistor, and *p* index refers to PNP transistor in model components)

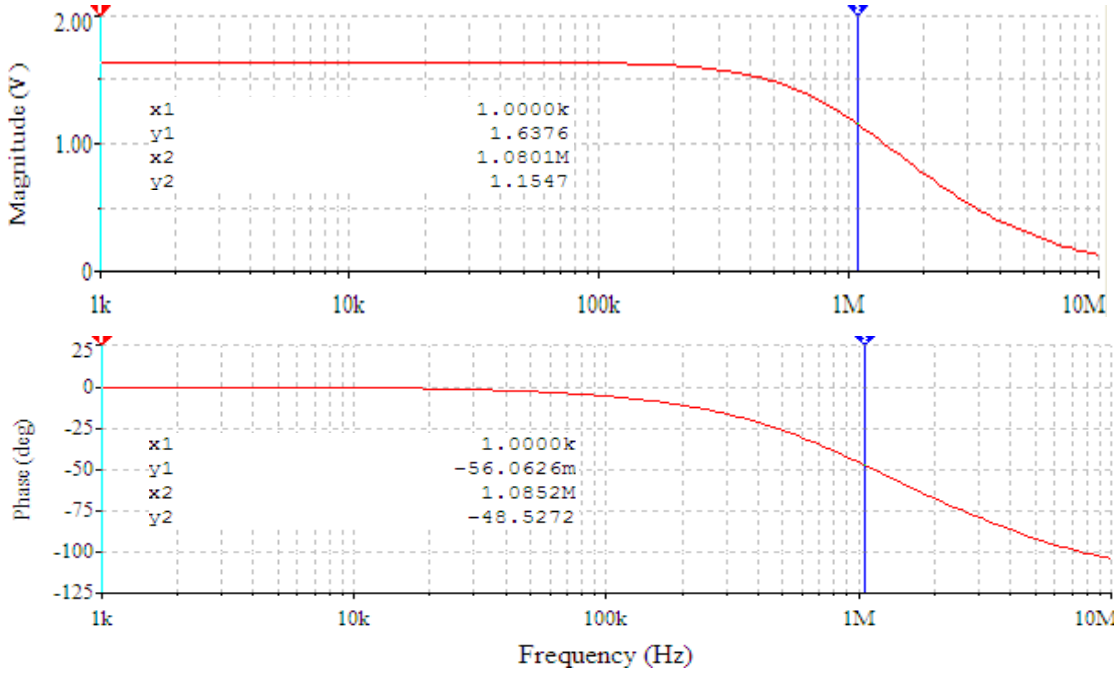

Figure 11 - Amplifier Frequency Response (VS) with BJTs replaced by their incremental model

Table 4 - Transresistance values

Transresistance		
Frequency (kHz)	Magnitude (kΩ)	Phase (deg)
1	32.75	- 0.056
10	32.75	- 0.56
100	32.61	- 5.59
1,000	23.92	- 46.07
10,000	2.61	- 104.03

6. AMPLIFIER TRANSIENT ANALYSIS

Various ***Multisim*** *Transient* analyses are then performed, in order to observe the effects of the sinusoidal input signal amplitude and frequency on the amplifier output voltage. In a first simulation, a low-amplitude (40µA peak-to-peak), 10 kHz signal is applied at the input of the amplifier (IENT). Both input and output signal are shown in Figure 12. Amplifier transresistance magnitude (|Rm|) can be calculated by the ratio between the value of ***dy*** (peak-to-peak value of V(Vs)) and peak-to-peak value of IENT, resulting in |Rm| = 1.3093/40.10^{-6} = 32.73 kΩ (as compared to 32.75 kΩ obtained from *AC* analysis, Table 2) . From these curves, it can be seen that input and output are in phase. Therefore, phase value of Rm is approximately zero (as compared to -0.56°, obtained from *AC* analysis, Table 2].

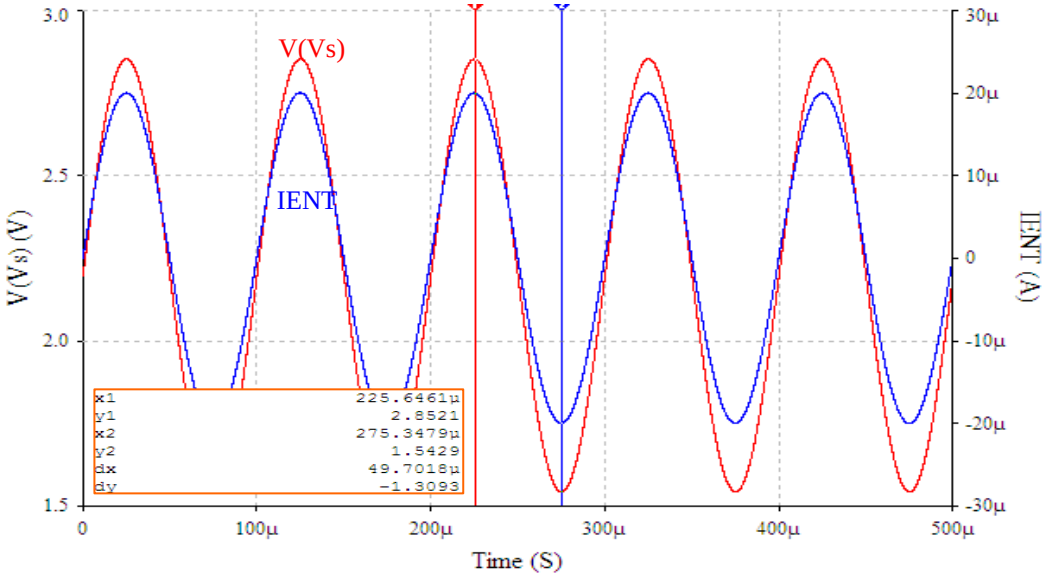

Figure 12 – Transient Analysis for a 10 kHz small-signal input

In a second run, the amplitude of input signal is kept small (40µA peak-to-peak), but its frequency is increased to 1 MHz, which is approximately the amplifier cut-off frequency. The results are shown in Figure 13. The new value of |Rm| is calculated as: = 0.958/40.10^{-6} = 23.95 kΩ (as compared to 23.94 kΩ from *AC* analysis, Table 2). Phase value of Rm (∠ Rm) can be calculated from the lower curves of Figure 13, where the horizontal difference between cursors (***dx***) and the period T can be used as follows: ∠ Rm = -360 • *dx* / T = -360 • 0.133. 10^{-6} / 10^{-6} = - 47.9° (as compared to - 46.0° from *AC* analysis, Table 2). These results confirm the cut-off condition at this frequency, since the output voltage value drops by √2 from its maximum in-band value. The third run is performed still keeping a small amplitude for the input signal (40µA peak-to-peak), but further increasing its frequency to 10 MHz. *Transient* analysis results in the waveforms shown in Figure 14. In this case |Rm| = 0.104/40.10^{-6} = 2.6kΩ (as compared to 2.61 kΩ from AC Analysis, Table 2) and the phase value ∠ Rm = -360 • *dx* / T = -360 • 0.029 10^{-6} / 10^{-7} = -104.4° (as compared to -104.1° from *AC* analysis, Table 2).

These *Transient* analysis simulations confirm that the effects of increasing input signal frequency beyond the amplifier cut-off limit are the decrease of the transresistance magnitude,

associated to the increase in the delay between output and input signals, given by the negative value phase of the transresistance. These results have been predicted in the AC amplifier analysis, as observed in Tables 2 and 3.

Another *Transient* analysis shows how the amplitude of input signal affects the amplifier output voltage. A low frequency (1kHz) with high level amplitude (240 µA peak-to-peak) IENT is applied to the amplifier input terminals. The resulting output waveform is shown in Figure 15. Response of the *Transient* analysis shows two regions of highly visible distortion, corresponding to IENT ≥ 105µA and IENT ≤ - 73µA. These values are close to the limits of Q1 cut-off and saturation regions, as presented in Figure 2. This case illustrates the occurrence of non-linearity when applying a high level input signal to the amplifier. The calculation of transresistance gain is not meaningful in this case, since it is a small-signal linear characteristic of the amplifier, and its calculation assumes that both input and output signals are purely sinusoidal. A last *Transient* analysis combines the effects of a high amplitude (large-signal) and high frequency input signal. In Figure 16, the Vs output waveform resulting from a 2MHz, 240 µA peak-to-peak IENT is displayed. Besides being affected in magnitude and phase, since it is operating beyond the cut-off frequency, the amplifier output is also distorted from sinusoidal shape, due to the high-level (large-signal) drive on transistor non-linear characteristic.

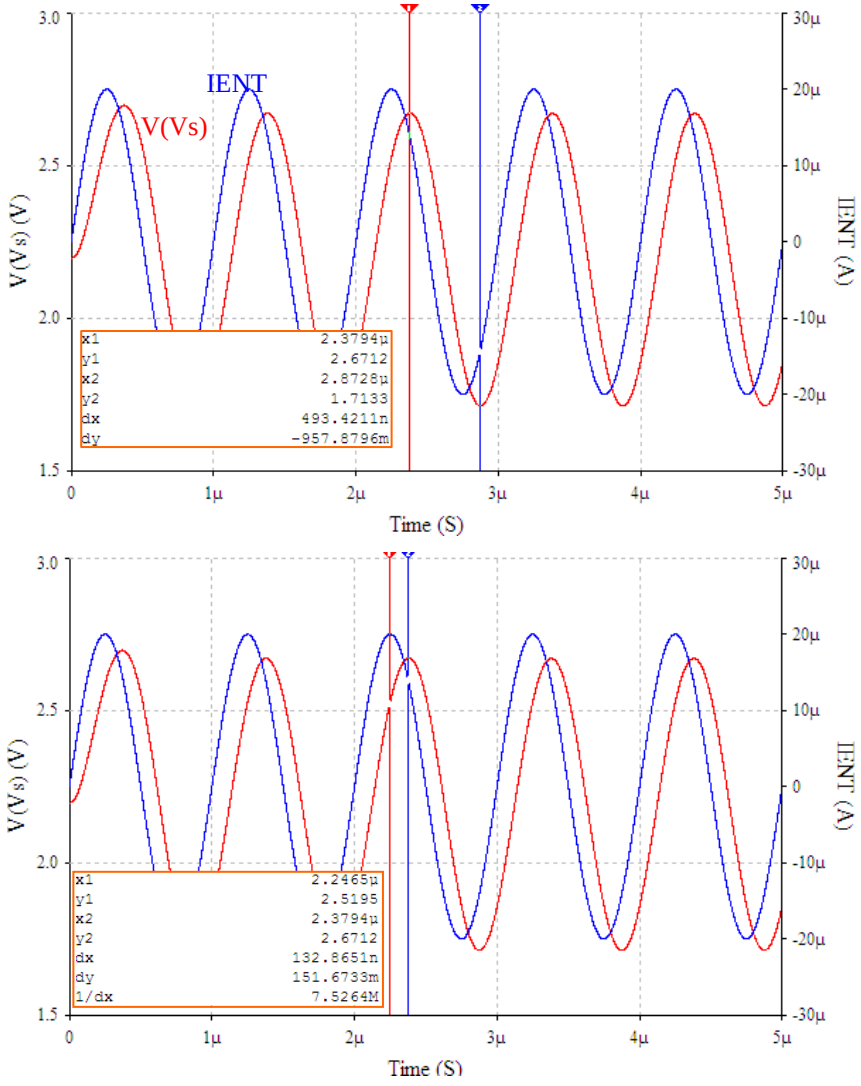

Figure 13 – Transient Analysis for a 1 MHz small-signal input

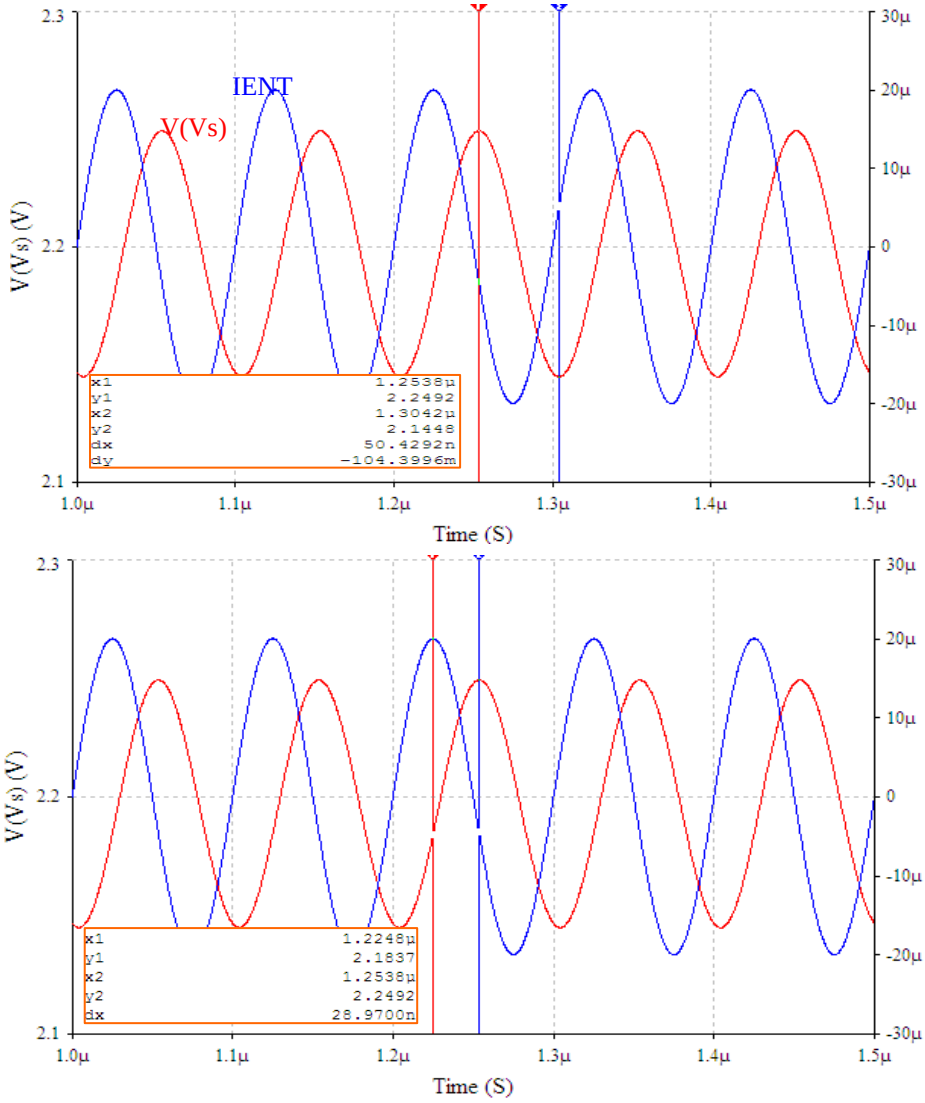

Figure 14 – Transient Analysis for a 10 MHz small-signal input

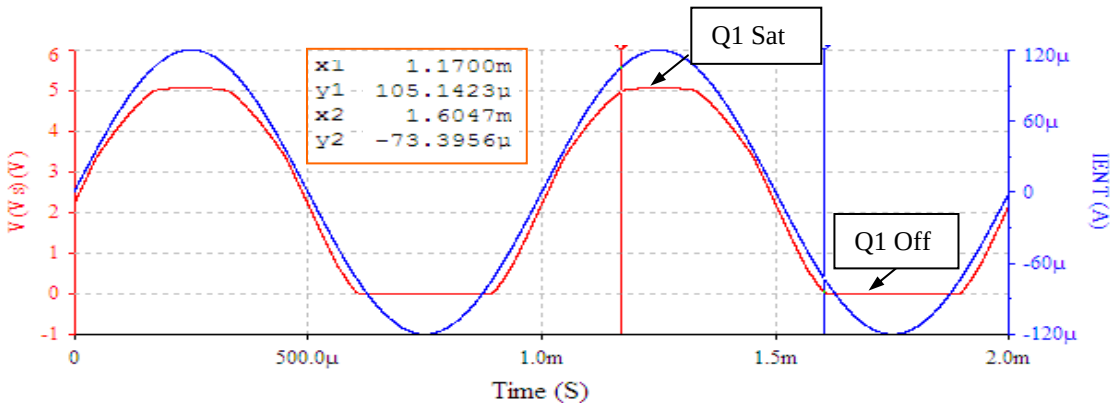

Figure 15 – Transient Analysis for a 1 kHz large-signal input

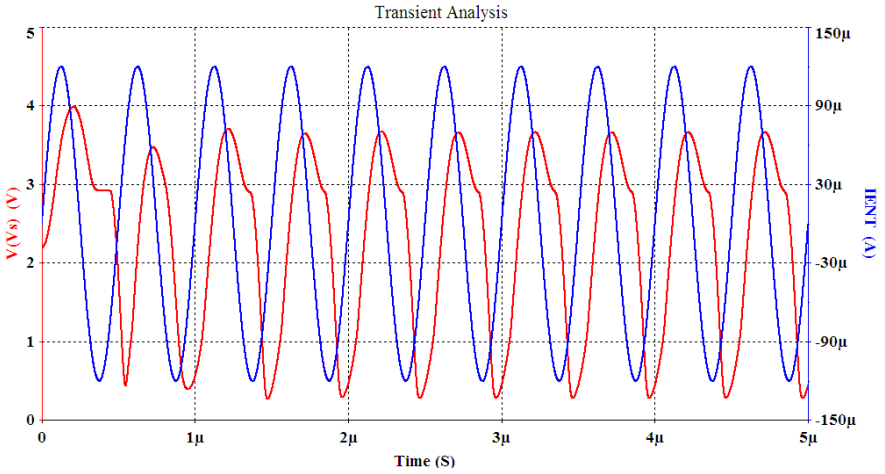

Figure 16 – Transient analysis for a 2 MHz large-signal input

7. AMPLIFIER FOURIER AND DISTORTION ANALYSES

The two other methods of analysis that can be of great practical interest in amplifier design are *Fourier* analysis and *Distortion* analysis. *Fourier* analysis produces a graph of harmonic components (magnitude and, optionally, phase) of a chosen node voltage waveform, resulting from Transient Analysis of the circuit. It also calculates the Total Harmonic Distortion (THD) as a percentage:

$$TDH = \frac{\sqrt{V_2^2 + V_3^2 + ...V_n^2}}{V_1} \times 100$$

where V_1 is the magnitude of fundamental component, and V_2, V_3 up to V_n are the magnitudes of harmonic components.

An example of the results obtained from *Fourier* analysis is presented in Figures 17 and 18. Figure 17 displays the amplifier output voltage waveform produced by a 500kHz, 120µA peak-to-peak IENT signal. Figure 18 is the spectral magnitude representation of Vs, containing also information on the harmonic components and the TDH value. It is interesting to notice that harmonic content is slightly visible in time domain (the output waveform is still nearly sinusoidal), whereas in frequency domain the harmonics appear, and the amplifier features a TDH equals to 14.63%.

Amplifier distortion can also be obtained from *Distortion* analysis (not available in ***Multisim Student*** version). The harmonic distortion can be analyzed by applying a pure sinusoidal signal with frequency *f* to the amplifier. ***Multisim*** calculates the desired node voltages at the harmonic frequencies *2f* and *3f* and displays the results against the input frequency *f*, as it sweeps across the user defined frequency range.

An example of *Distortion* analysis applied to the output voltage VS of the Darlington Amplifier is illustrated in Figures 19 and 20 (second and third harmonic distortion, respectively, for IENT= 120µA peak-to-peak). From these curves, the designer can easily predict frequency points of maximum amplifier harmonic distortion.

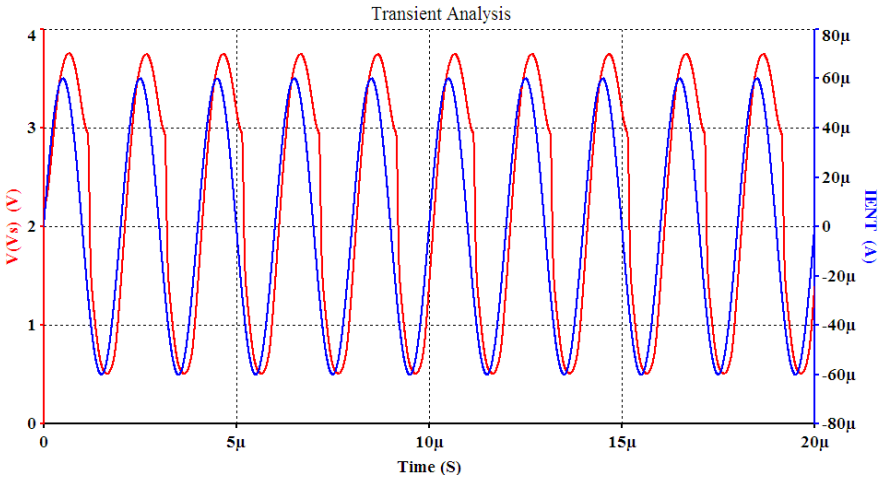

Figure 17 – Vs Transient Analysis for IENT = 120 µA peak-to-peak, 500 kHz

2	DC component:	2.19314				
4	THD:	14.63 %				
8	Harmonic	Frequency	Magnitude	Phase	Norm. Mag	Norm. Phase
9	1	500000	1.72235	-29.219	1	0
10	2	1e+006	0.138746	64.6739	0.0805564	93.8931
11	3	1.5e+006	0.137466	-110.19	0.0798128	-80.974
12	4	2e+006	0.102753	16.5255	0.0596587	45.7447
13	5	2.5e+006	0.0694612	158.673	0.0403293	187.892
14	6	3e+006	0.0610409	-37.497	0.0354405	-8.2778
15	7	3.5e+006	0.0531566	100.425	0.0308628	129.644
16	8	4e+006	0.0440418	-111.93	0.0255708	-82.712
	9	4.5e+006	0.0383739	38.8792	0.02228	68.0984

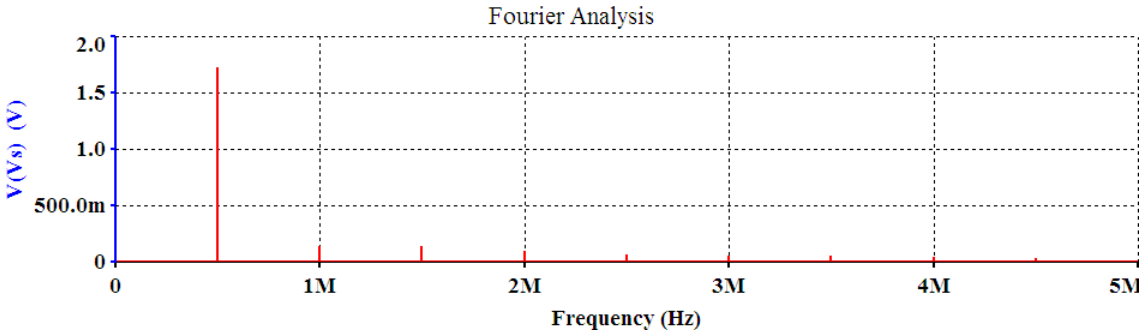

Figure 18 – Results of Fourier Analysis applied to waveform of Figure 17

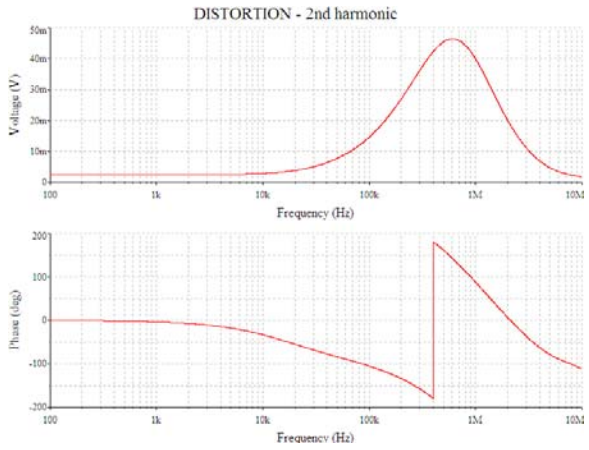

Figure 19 – Results of second harmonic Distortion Analysis

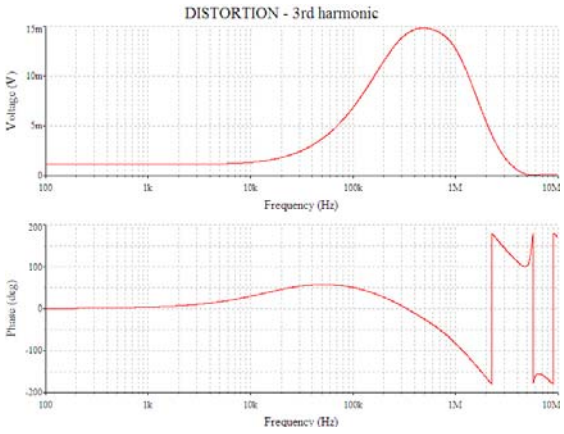

Figure 20 - Results of third harmonic Distortion Analysis

8. COMPARING ANALYSIS METHODS AND TRANSISTOR MODELS

In any electronic circuit, the bias point is the initial value for all other calculations. In manual design, it is normally restricted to some desired DC values of voltages and currents along the circuit. However, when using a simulator like ***Multisim***, the *DC Operating Point* analysis also results in the parameter values of device models employed in the circuit (BJTs in our case). As shown in this tutorial, such values are fundamental when building linear DC (Figure 4) or incremental AC (Figure 9) equivalent models for these electronic components. Simulations help the students to become conscious about the limitations of all these types of models and how they are treated in each analysis method. The most extensive model is the non-linear Ebers-Moll, contained in the ***Multisim*** Database, with its parameters extracted from real commercial devices. This model can be used for all analysis: *DC*, *AC* and *Transient*, since they include all appropriate linear and non-linear circuit components, which are necessary to predict amplifier performance under several different conditions. Some points about models and methods of analysis should be disclosed to the students, and this study case is a good opportunity for that:

- In *DC* analysis, all capacitors and inductors in the non-linear model are replaced by open and short circuits, respectively, but the model contains resistances and dependent sources which are described by non-linear equations that can mimic the electronic device real operation. For this reason, the DC transfer curve obtained (Figure 3) presents the cut-off active and saturation regions of the transistor operation. On the other hand, when composing a DC linear model (Figure 4) from the parameters calculated in the DC Operating Point analysis, the amplifier transfer characteristic results purely linear (Figure 6), which is unreal. Such simplified model however can safely be used to predict small-signal AC operation of the amplifier, around the bias point, within the region where both curves almost coincide (Figure 6). That means that linear models are useful when the bias point is properly set, and the amplitude of the input signal is small enough to guarantee that transistors are operating in their active region, and signal variation does not surpass the linear region of this curve.
- In *AC* analysis, all DC sources are inactivated and sinusoidal steady-state operation of the circuit around the quiescent point is assumed. It is always a linear frequency-domain analysis. In this case, ***Multisim*** replaces the original non-linear model by a linear incremental model, similar to that shown in Figure 9, using the parameters calculated in the *DC Operating Point* analysis. For this reason non-linear effects caused by large-signal driving cannot be predicted in this analysis. The results are magnitude and phase of voltages and currents in function of frequency, and are valid only under input small-signal restrictions. This explains why the amplifier frequency responses obtained with the non-linear models and with the linear π-hybrid AC model (Figure 9) practically coincide (Figure 8 with Figure 11, Table 2 with Table 3).
- In the *Transient* analysis, all DC and time-varying sources are activated, the complete non-linear model is used and a time-domain analysis is performed. Therefore, it is the only analysis that can simulate circuit operation under various signal waveforms, with different amplitude and frequencies, taking into account effects of capacitances and inductances and all kinds of non-linearities. For each condition, ***Multisim*** fits model parameters according to the level of the driving signal and calculates voltage and currents in function of time. For a better prediction of amplifier performance, only the non-linear model should be used in this analysis. Figures 12 to 16 illustrate various conditions of amplifier operation: low-frequency small-signal, high-frequency (beyond cut-off) small-signal, low-frequency large-signal and high-frequency large-signal. Since Darlington Amplifier presents a low-pass frequency transresistance characteristic (Figure8), it can be observed that, as long as input signal is kept with small amplitude, effects of increasing frequency beyond the cut-off limit are the drop in

transresistance magnitude associated to the increase in transresistance delay (as shown in Figure 14). When the input drive is raised, BJTs are forced into cut-off and saturation regions, producing distortive effects on the amplifier output voltage (Figure 15), which is no longer sinusoidal. When high-frequency large-signal input is applied to the amplifier, a combination of all these effects can be observed (Figure 16).

- The *Fourier* analysis and *Distortion* analysis convert waveforms from a *Transient* analysis to the frequency domain, calculating their harmonic content. They employ the complete non-linear model, being a useful tool to predict non-linear effects in steady-state circuit operation, as such prediction is not possible in linear AC analysis, for the reasons explained above. The Total Harmonic Distortion (THD) is a very useful factor to evaluate amplifier features. The lower the THD, the better is the amplifier quality, meaning that it introduces less distortion while amplifying the input signal. Some times distortion effects are hardly noticed in the waveforms obtained after *Transient* analysis. The appearance of harmonics in the signal spectrum, visualized through *Fourier* analysis, as well as second and third harmonic magnitude and phase variation with frequency, obtained through *Distortion* analysis, are powerful results in amplifier practical design procedures.

9. CONCLUSIONS

In this Tutorial, the study of a Darlington Amplifier provides a valuable means for early year Electrical Engineering students in understanding and assimilating basic concepts and procedures of the design and analysis of electronic circuits. ***Multisim*** proved to be a powerful and friendly tool for simulating *DC*, *AC* and *Transient* behavior of the circuit, also providing in its library the required models for real BJT devices. Transfer characteristic, model parameter extraction, repeated simulations under several signal conditions, *Fourier* and *Distortion* analyses are easily run and produce illustrative results that greatly contribute to the process of learning electronic circuits.

Acknowledgment

The authors would like to thank Prof. L.Q. Orsini, who firstly proposed the Darlington Amplifier simulation exercise to the Electrical Engineering students at Escola Politécnica, University of São Paulo, and from whom they have learnt a great deal about device modeling and electrical circuit analysis and simulation. The authors also acknowledge *National Instruments* for providing the ***Multisim*** software licence.

REFERENCES

National Instruments, http://www.ni.com/multisim/

SEDRA, A.S.; SMITH, K.C. **Microelectronic Circuits**, 4th Ed., Oxford University Press, 1997.

ANTOGNETTI, P.;MASSOBRIO,G. **Semiconductor Device Modelling with SPICE**, McGraw-Hill Book Company, 1988.